

**IN THE CLAIMS**

1. (Original.) A method for reducing distortion of a signal applied to an input of a circuit having a parasitic capacitance, comprising the steps of:  
detecting a direction of change in voltage of said input signal; and  
introducing a current to said parasitic capacitance to compensate for current of said input signal charging said parasitic capacitance responsive to detection of a positive edge of said input signal.
2. (Previously amended.) The method of claim 1, wherein said signal is applied to an input of said circuit.
3. (Previously amended) A method for reducing distortion of a signal applied to an input of a circuit having a parasitic capacitance, comprising the steps of:  
detecting a direction of change in voltage of said input signal; and preventing discharge of said parasitic capacitance into the input of said circuit responsive to detection of a negative edge of said input signal.
4. (Withdrawn.)
5. (Previously amended.) Apparatus for reducing distortion of a signal applied to an input of a circuit operating at high frequency and having a parasitic capacitance, comprising:

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a detection circuit for detecting a change in voltage of said input signal coupled to said input; and

a correction circuit coupled to said detection circuit for compensating for current from said input signal diverted to said parasitic capacitance due to a positive edge of said input signal.

6. (Original) The apparatus of claim 5, wherein said detection circuit includes a capacitance.

7. (Canceled.)

8. (Previously amended.) Apparatus for reducing distortion of a signal applied to an input of a circuit operating at high frequency and having a parasitic capacitance, comprising:

a detection circuit for detecting a change in voltage of said input signal coupled to said input; and

a correction circuit coupled to said detection circuit for compensating for current from said parasitic capacitance to be added to said input signal due to a negative edge of said input signal.

9. (Original) The apparatus of claim 8, wherein said detection circuit includes a capacitance.

10. (Canceled.)

11. (Withdrawn.)

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12. (Original). A method for reducing distortion of a signal applied to an input of a circuit having a parasitic capacitance, comprising the steps of:  
detecting a direction in change in voltage of said input signal; and  
introducing a current to said parasitic capacitance to compensate for distortion of said input signal due to said parasitic capacitance responsive to detection of a positive edge of said input signal.

13. (Presently amended) A method for reducing distortion of a signal applied to an input of a circuit having a parasitic capacitance, comprising the steps of:

detecting a direction of change in voltage of said input signal; and  
preventing introduction of a current from said parasitic capacitance into said input signal responsive to detection of a negative positive edge of said input signal.

14. (Withdrawn.)

15. (Withdrawn.)

16. (Withdrawn.)

17. (Withdrawn.)

18. (Previously added.) The method of claim 1 wherein the parasitic capacitance is across said input and ground, said introducing step including introducing the current to said input.

19. (Previously added.) The method of claim 3 wherein the parasitic capacitance is across said input and ground, the step of preventing discharge including introducing the current to said input.

20. (Previously added.) The apparatus of claim 9 wherein said parasitic capacitance appears between said input and ground.

*11/11/01*  
21. (Withdrawn.)

22. (Previously added.) The apparatus of claim 12 wherein said parasitic capacitance appears between said input and ground.

23. (Previously amended.) The method of claim 13 wherein the parasitic capacitance is across said input and ground, the step of preventing discharge including introducing the current to said input.

24. (Withdrawn.)

25. (Previously added.) The apparatus of claim 6 wherein the capacitance of the detection circuit has one terminal directly connected to one terminal of the parasitic capacitance.

26. (Previously added.) A method for reducing distortion of a signal applied to an input of a circuit having a parasitic capacitance, comprising the steps of:

detecting a direction of change in voltage of said input signal; and

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introducing a current to said parasitic capacitance to compensate for current of said input signal charging said parasitic capacitance responsive to detection of a positive edge of said input signal, thereby eliminating a need for an additional parasitic capacitance to reduce distortion.

27. (Previously added.) A method for reducing distortion of a signal applied to an input of a circuit having a parasitic capacitance, comprising the steps of:

detecting a direction of change in voltage of said input signal; and preventing discharge of said parasitic capacitance into the input of said circuit responsive to detection of a negative edge of said input signal, thereby eliminating a need for an additional parasitic capacitance to reduce distortion.